Amendments to the Specification:

After paragraph 27, add a new paragraph 27.1:

[0027.1] FIG. 4 illustrates in block diagram form a delay-difference detector circuit according to one embodiment of the invention

After paragraph 38, add new paragraphs 38.1 and 38.2:

[0038.1] With reference now to Fig. 4, there is shown an alternate embodiment of the delay-difference detector 6 of Fig. 2, comprising combinatorial-logic circuit 7 receiving the output signals A and B from circuits 2 and 3 and generating the output signals S11 and R11 to be supplied to sequential-logic circuit 11 and generating the output signals S12 and R12 to be supplied to sequential-logic circuit 12 and generating the output signals S13 and R13 to be supplied to sequential-logic circuit 13 and generating the output signals S14 and R14 to be supplied to sequential-logic circuit 14. Delay-difference detector 6 further comprises combinatorial-logic circuit 8 receiving the output signals C and D from circuits 4 and 5 and generating the output signals S15 and R15 to be supplied to sequential-logic circuit 15 and generating the output signals S16 and R16 to be supplied to sequential-logic circuit 16 and generating the output signals S17 and Ri7 to be supplied to sequential-logic circuit 17 and generating the output signals S18 and R18 to be supplied to sequential-logic circuit 18.

[0038.2] Sequential-logic circuit 11 generates an output signal Q11 (and possibly an inverse output signal) to be supplied to low pass filter 21, sequential-logic circuit 12 generates an output signal Q12 (and possibly an inverse output signal) to be supplied to low pass filter 22, sequential-logic circuit 13 generates an output signal Q13 (and possibly an inverse output signal) to be supplied to low pass filter 23, sequential-logic circuit 14 generates an output signal Q14 (and possibly an inverse output signal) to be supplied to low pass filter 24, sequential-logic circuit 15 generates an output signal Q15

(and possibly an inverse output signal) to be supplied to low pass filter 25, sequential-logic circuit 16 generates an output signal Q16 (and possibly an inverse output signal) to be supplied to low pass filter 26, sequential-logic circuit 17 generates an output signal Q17 (and possibly an inverse output signal) to be supplied to low pass filter 27, and sequential-logic circuit 18 generates an output signal Q18 (and possibly an inverse output signal) to be supplied to low pass filter 28. An output of low pass filters 21 – 28 is coupled to an input of analog adder/subtractor 9.